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Author(s): Alatise, O. Kennedy, I. Petkos, G. Koh, A.
Article Title: Reliability of Repetitively Avalanched Wire-Bonded Low-Voltage Discrete Power Trench n-MOSFETs
Year of publication: 2010
Link to published article:
http://dx.doi.org/10.1109/TDMR.2010.2102026
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Reliability of Repetitively Avalanched Wire-bonded Low Voltage Discrete Power Trench N-MOSFETs

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Abstract –This report for the first time investigates the reliability wire-bonded low voltage discrete power trench n-MOSFETs that have been subjected to repetitive unclamped inductive switching (RUIS). Automotive MOSFETs driving inductive loads may be subjected to RUIS; hence there is a need to characterize the failure mechanisms in such applications. The failure mechanism of repetitively avalanched wire-bonded MOSFETs is shown to be wirebond lift-off and source metal degradation/fatigue due to thermo-mechanical stress cycling. Temperature excursions from avalanche pulses cause thermo-mechanical stresses on the wirebond/source metal interface as a result of differences in thermal expansion coefficients between silicon and aluminum. Trench MOSFETs exhibited an average of 10% increase in on-state resistance due to source metal fatigue after 100 million cycles of repetitive avalanche. The number of cycles to failure is investigated as a function of the avalanched induced temperature changes and is shown to follow the Coffin-Manson law. These results are important for designers of automotive systems since they are capable of predicting the long term reliability of wire-bonded discrete power semiconductor components.

Index Terms: Coffin-Manson, Repetitive Avalanche, Trench MOSFETs, Wirebonds

I. INTRODUCTION

Discrete power MOSFETs are increasingly playing an important role in automotive electronics such as motor control where inductive loads are driven by the power devices. As a consequence, the ability of the MOSFET to withstand instances of unclamped inductive switching (UIS) is an important performance metric i.e. the ruggedness of the MOSFET. When the MOSFET is switched on, energy is stored in the magnetic field of the inductive load and when the MOSFET is switched off, the inductive load dissipates energy into the MOSFET by driving it into avalanche mode conduction. In some designs, the MOSFET is protected from avalanche pulses by using free-wheeling diodes (FWD); however, this is not always the case as the cost and design may not permit. MOSFETs can be thermally destroyed through parasitic bipolar latch-up if the energy of the UIS pulse is sufficient to trigger the parasitic bipolar by forward biasing the emitter-base junction. The parasitic bipolar transistor is activated when there is a voltage drop within the p-body of the MOSFET sufficient to cause a potential difference between the p-body and the n^+ source that is greater than the in-built source-body pn diode voltage [1]. This is the case when there is a large hole current in the p-body generated from impact ionization and elevated temperatures increase the body resistance through phonon scattering. However, well designed MOSFETs today have source-body junction designs that reduce the risk of BJT latch-up and extensive characterization of the safe-operating-area (SOA) on datasheets informs designers of the limitations of the power discretes. The SOA on MOSFET datasheets usually shows the avalanche power density and duration that the MOSFET is capable of withstanding. However, there hasn't been as much characterization of the impact repetitive UIS of power pulses within the SOA on the reliability of power devices. This is probably because not many designs have demanded such repetitive UIS requirements from their power discretes. The increasing use of advanced MOSFETs in automotive applications makes this a necessity.

In avalanche mode conduction, the source-drain voltage rises to the breakdown voltage (B_{VDSS}) as the avalanche current (I_{AV}) flows through the device. As a result, a large amount of power ($B_{VDSS}\cdot I_{AV}$) is dissipated through the device. The junction temperature (T_J) of the MOSFET increases as the power pulse passes through the device. The magnitude of the temperature rise depends on the size of the inductor (L), the avalanche current, the breakdown voltage rating of the MOSFET and the MOSFET's transient thermal impedance response (Z_{TH}). Fig. 1(a) shows a simple schematic diagram of a power MOSFET driving an inductive load whereas Fig. 1(b) shows idealized timing diagrams of gate voltage (V_{GS}), the drain voltage (V_{DS}), the drain current (I_D), the avalanche power (P) and the junction temperature [2]. From zero to time t_1, the gate voltage of the power MOSFET is off, the drain current is zero and the drain source voltage is tied to the power supply voltage (V_S). As a consequence there is no power dissipated in the power MOSFET according to Fig. 1(b) and hence no temperature rise. In reality, there is a drain leakage current (I_{DSS}) that is generated due to band-to-band tunneling and subthreshold leakage hence some power is dissipated because of this. This leakage current increases rapidly with temperature hence the off-state power dissipation of MOSFETs in high temperature applications cannot be ignored as insignificant. From time t_1 to t_2, the power MOSFET is switched on thereby causing the drain current to increase linearly and store energy in the magnetic fields of the inductor. The drain voltage of the power MOSFET falls to zero in Fig. 1(b) but in reality, it falls to $I_{DS}\cdot R_{DSON}$ (which is very low for a well designed low voltage trench MOSFET). The power dissipated between periods t_1 and t_2 in Fig. 1(b) is shown as zero however in reality it is $I_{DS}^2\cdot R_{DSON}$ and is usually referred to as the conduction loss. Also, the timing diagrams in Fig. 1(b) assumes that the gate voltage and drain voltage rise and fall instantaneously, however, the need to charge the gate-source and gate-drain capacitances means that there will be a finite switching time and hence a turn-on power loss associated with that time. This switching loss becomes increasingly significant

as the switching frequency of the MOSFET increases. From time t_2 to t_3, the power MOSFET is switched off, thereby causing the drain current to ramp down. Again, the turn-off switching loss is ignored by assuming instantaneous switching. In this duration, the drain-source voltage rises to the B_{VDSS} and a considerable amount of power ($B_{VDSS} \cdot I_{AV}$) is dissipated through the MOSFET. This power, which is represented as a shaded triangle in Fig. 1(b), causes a temperature excursion between time t_2 and t_3.

Repetitive temperature excursions associated with each avalanche pulse cause the metallic wirebonds, the source metal and the silicon chip to undergo thermal cycling. Differences in thermal expansion coefficients between the source metal, silicon chip and wirebonds generate thermo-mechanical stresses that cause long term structural reliability concerns. Previous studies have investigated the impact of thermal cycling on the long-term structural integrity of the joints in wire-bonded power devices [3] and the structural integrity of direct-chip attach assemblies where silicon chips have different thermal expansion coefficients with laminated substrates [4]. Other studies have also been reported on automotive planar MOSFETs used in anti-lock braking systems that are subject to cyclical temperature excursions and thermo-mechanical stresses from current cycling [5]. The purpose of this article is to shed further light on long term reliability constraints in wire-bonded power MOSFETs that are subjected to numerous avalanche pulses in automotive applications.

II. EXPERIMENTAL PROCEDURES

The low voltage trench MOSFETs under investigation have rated B_{VDSS} of 20 V (measured as 25 V) and room temperature (25 °C) threshold voltages (V_{GSTH}) of 2.5 V. Three different sizes of MOSFETs (25mm^2, 49 mm^2 and 58 mm^2) were investigated. The starting substrate was grown with an epi doping and thickness designed for 20 V rated devices. The

size of the MOSFET is defined by the dimensions on the mask layers designed for photolithography. Trenches with a depth of 1.5 μm were etched and a 76 nm silicon dioxide gate dielectric was grown by thermal oxidation. Polysilicon gates were deposited and planarized after which boron p-body implants and phosphorus n^+ source implants were performed successively. TEOS passivation was deposited and contact windows for the source metal were etched and filled with aluminum. The 25 mm^2 MOSFETs were soldered on copper lead-frames and packaged in standard TO-220 packages with 3 source wirebonds soldered on the aluminum source metal and 1 gate wire bonded on the aluminum gate. The 49 mm^2 and 58 mm^2 MOSFETs were assembled in custom-made electrical modules as bare-dies assemblies with 8 source wires. Fig. 2 shows a cross-section of the processed device with the TEOS passivation, trench polysilicon, gate dielectric and silicon substrate. Fig. 3(a) shows a picture of the de-capped 25 mm^2 MOSFET whereas Fig. 3(b) shows that of the 49 mm^2 MOSFET. The repetitive avalanche test gear consists of high voltage charging MOSFETs, an inductor, a pulse generator and a power supply. Fig. 4 shows a schematic of the circuit diagram of the repetitive avalanche test gear. The pulse generator switches on the charging MOSFETs which store energy in the inductor. When the charging MOSFETs are switched off, the inductor dissipates the stored energy into the DUT. The charging MOSFETs have B_{VDSS} much higher than the DUT so as to ensure that avalanche current is conducted through the DUT. The gate drive of the charging MOSFETs is used to set the avalanche current whereas the inductor is used to set the avalanche pulse duration.

The junction temperature response of the power MOSFET to the avalanche pulse is calculated using an empirically derived transient thermal impedance curve. An example of the junction temperature response is shown in Fig. 5 which is the temperature response of a 25 mm^2 20 V rated power MOSFET subjected to 1.28 J of avalanche energy (a power density of 247 W/mm^2). As can be seen from Fig. 5 the maximum junction temperature (T_{JMAX}) is

approximately 180 °C.

III. RESULTS AND DISCUSSION

Discrete power trench MOSFETs have been avalanched cycled to destruction under different test conditions. Different avalanche currents were used in the repetitive ruggedness characterization of the different sized MOSFETs. For each test condition, 10 devices were tested simultaneously hence the results presented are averaged over the devices. The devices were screened using production tests and single shot ruggedness screening tests so as to ensure that maverick devices were not included in the test population. The repetitive ruggedness tests were performed until the devices were destroyed. Table 1 shows the results for the 25 mm^2 MOSFET in TO-220 and the 49 mm^2 and 58 mm^2 MOSFETs in custom made packages. The avalanche current, power density, energy and temperature rise is calculated for each set of experiments.

Cross-sectional images as well as pictures of de-capped devices have been obtained from un-tested and tested devices. Fig. 6(a) and 6(b) shows the comparison between the cross-sectional images of the source metal of a tested and an un-tested device. What is immediately obvious in Fig. 6 is the difference in the quality of the source metal with the tested devices showing clear symptoms of fatigue. Previous reports have shown a similar signature in thermally cycled metallic thin films where there is a clear disintegration in the structural constitution of the metal through the formation of hillocks [6]. The formation of hillocks on thermally cycled aluminum thin films was reportedly due to the imposition of stresses in the film arising from differences in the thermal expansion coefficients between aluminum and silicon. It was reported that grain boundary separation could result from thermal cycling as compressive and tensile stresses alternate between heating and cooling. Fig. 6 shows clear signs of grain separation; hence, it is thought that the same thermo-mechanical mechanism is

active. A similar observation of metallic film degradation was made on the emitter metal of a silicon insulated gate bipolar transistor (IGBT) that had been subjected to thermo-mechanical stress cycling from repetitive short circuit tests [7]. Other reports in literature have identified wirebond cracking and liftoff as active failure modes in power discrete components that undergo thermo-mechanical stress cycles [8-13].

As a result of the degradation in the source metal shown in Fig. 6, there is an increase in the measured drain-source resistance (R_{DSON}) with increasing avalanche cycles. Fig. 7 shows R_{DSON} as a function of the number of avalanche cycles for sixteen 25 mm^2 power MOSFETs repetitively avalanched at 160 A. There is an average 10% increase in R_{DSON} which can be attributed to the degradation in the source metal structure as well as the wirebond to source metal interface. Other reports in literature have also sighted increased film resistance as a result of metal fatigue due to thermo-mechanical stressing [14].

Fig. 8(a) shows the image of the tested 25 mm^2 MOSFET in TO-220 de-capped with a severe burn on the middle wirebond whereas Fig. 8(b) shows that of the 49 mm^2 MOSFET also with a burn mark. When failure analysis was done on the MOSFETs, it was observed that the un-burnt wirebonds were loose and lifted off the source metal. To check the relationship between the lifted wirebonds and the burnt wire, MOSFETs were avalanche cycled and taken out for failure analysis before destruction. Cross-sectional images were taken across the wirebonds so as to investigate the structural integrity of the wirebond to source metal interface. This was done for MOSFETs repetitively avalanched to 2 million cycles and 20 million cycles in an effort to investigate the structural condition of the wirebonds as a function of avalanche cycles. Fig. 9(a) shows the cross-sectional image of the wirebond/MOSFET interface of the device that has undergone 2 million cycles of repetitive avalanche whereas Fig. 9(b) shows that of the device that has undergone 20 million cycles. Fig. 9 shows where crack propagation from thermo-mechanical cycling manifests itself. It can be seen from Fig. 9

that the cracks in the wirebonds of the MOSFETs that have undergone 20 million cycles of repetitive avalanche are longer in length when compared to those that have undergone 2 million cycles. Fig. 10 shows a schematic diagram of the wire-bonded MOSFET highlighting the three critical components in thermo-mechanical stress cycling which are the aluminum wirebond, the aluminum source metal and the silicon die. The heat generated from the avalanche power dissipated in the MOSFET exists in approximately in the first few micrometers of silicon under the source metal because the breakdown voltage of the MOSFET is sustained between the source and the drain along the 1.5 μm deep trench. Because of the lower coefficient of thermal expansion in silicon, this heat is not dissipated as quickly as it would be in the aluminum source wirebonds hence the source metal is at a constantly elevated temperature compared with the wirebonds. The different thermal boundary conditions between the source wirebonds and the source metal causes different rates of expansion and contraction, hence in-built stresses cause crack generation and propagation along the interface of the 2 metals. Wirebond liftoff has also been reported as a failure mechanism in silicon IGBTs that have been subjected to repetitive short circuit tests [7].

These tests show that temperature excursions from the avalanche pulses cause mechanical stresses that arise because of differences in the co-efficient of thermal expansion in aluminum and silicon. The length of the cracks in the wirebond/source metal interface increases with the number of cycles thereby causing the wirebonds to shear off once the critical length of the crack has been reached. Because of differences in the wirebonds, crack generation and propagation is not identical across all wirebonds hence, wirebond liftoff is not simultaneous among all wirebonds. The burn in Fig. 8 shows that most of the current flows through the intact wirebond when the other wirebonds have lifted thereby causing a rapid rise in current density and a corresponding rise in the localized temperature around the wirebond. Failure subsequently occurs when the temperature surge around the intact wirebond cannot be

sustained as it exceeds the limit of the metal and the silicon.

Fracture generation and creep in single phase metallic materials subjected low cycle fatigue has been reported to routinely follow the Coffin-Manson relation [15]. The Coffin-Manson relation is an empirical relation that expresses the number of cycles to failure as a function of the cyclic plastic deformation and is usually expressed as

$$NCTF \cdot \Delta\varepsilon^{\beta} = C$$

where *NCTF* is the number of cycles to failure, $\Delta\varepsilon$ is the plastic strain (which is dependent on the change in temperature ΔT), β is an empirical exponent and *C* is a proportionality constant of the material. Reports in literature have used the Coffin-Manson relation to characterize wirebond reliability in thermo-mechanically cycled power devices [4, 16]. The results in table 1 have been plotted in Fig. 11 so as to investigate whether wire-bond lift-off in repetitively avalanched power MOSFETs follows the Coffin-Manson relation. The points in Fig. 11 show the measurement points in table 1 whereas the line of best fit is of the equation $NCTF = 5\times10^{19}\Delta T^{-6.4}$. Fig. 11 shows that the fracture mechanics of wirebonds under thermo-mechanical stress cycling from repetitive avalanche follows the Coffin-Manson relation. This is important for the purposes of estimating the reliability of wire-bonded power semiconductor devices in automotive applications where repetitive avalanche is an operating condition.

IV. SUMMARY

Discrete power trench MOSFETs have been repetitively avalanched to destruction with pulses within the safe-operating-area of the device. The failure mode is shown to be wirebond lift-off due to the crack generation and propagation along the source wire to source metal interface as

a result thermo-mechanical stresses. As a consequence of some source wirebonds losing electrical contact with the source metal, there is a localized current density and temperature surge in the intact wirebonds thereby causing localized failure through melting metal/silicon. Cross-sectional images of the source metal on tested MOSFETs show degradation in the structural constitution of the metal which is indicative of fatigue. This degraded source metal causes the measured on-state resistance to increase with the number of cycles. Cross-sectional images of the wirebond to source metal interface show cracks generating and propagating along the interface with the crack length increasing with the number of cycles on repetitive avalanche. Extensive tests on 25 mm^2, 49 mm^2 and 58 mm^2 power MOSFETs at different avalanche currents show that the number of cycles as a function of the electro-thermal temperature rise follows the Coffin-Mason relation. These results are important especially for automotive MOSFETs that drive inductive loads.

REFERENCES

[1] I. Pawel, R. Siemieniec, M. Rosch, F. Hirler, and R. Herzer, "Experimental study and simulations on two different avalanche modes in trench power MOSFETs," *IET Circuits Devices Syst.*, vol. 1, no. 5, pp. 341–346, Oct. 2007.

[2] A. Koh, Power MOSFET Single and Repetitive Avalanche Ruggedness Rating, 2003, Application note AN10273.

[3] T. Matsunaga and S. Sudo, "Evaluation of fatigue life reliability and new lead bonding technology for power modules," *Mitsubishi Electr. Adv.*, vol. 113, pp. 13–16, 2006, Technical Reports.

[4] V Getkin, A Bar-Cohen, S Witzman "Coffin-Manson based fatigue analysis of underfilled DCAs" *IEEE Transaction on Components, Packaging and Manufacturing Technology*, vol. 21, no. 4, pp. 577-584, Dec. 1998.

[5] A. Testa, S. D. Caro, S. Panarello, S. Patane, R. Letor, S. Russo, S. Poma and D. Patti, "Stress analysis and lifetime estimation on power MOSFETs for automotive ABS systems," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 1169–1175.

[6] C Santoro, "Thermal cycling and surface reconstruction in aluminum thin films", *J. Electrochem. Soc*, vol. 116, no. 3, pp. 361-364, 1969.

[7] M Arab and Z Khatir, "Investigations on ageing of IGBTs under repetitive short-circuit operations", *Power electronics Europe*, issue 5, pp. 22-24, 2008.

[8] W. Loh, M. Corfield, H. Lu, S. Hogg, T. Tilford, and C. Johnson, "Wirebond for power electronic modules—Effect of bonding temperature," in *Proc. Int. Conf. Thermal, Mech. Multi-Phys. Simul.* Experiments Microelectron. Micro-Syst., EuroSime, 2007, pp. 1–6.

[9] A Hamidi, N Beck, K Thomas and E Herr, "Reliability and lifetime evaluation of different wirebonding technologies for high power IGBT modules" *Microelectronics Reliability*, vol. 39, issues 6-7, pp. 1153-1158, 2008.

[10] T Matsunaga and Y Uegai, "Thermal fatigue life evaluation of aluminum wire bonds "Reliability of wire-bonding and solder joint for high temperature operation of power semiconductor device", *Microelectronics Reliability*, vol. 47, no. 12, pp. 2147-2151, 2007.

[11] J Calata, L Guo-Quan and C Luechinger, "Evaluation of interconnect technologies for power semiconductor devices" *The 8th intersociety conference on thermal and thermomechanical phenomena in electronic systems*, 2002, pp. 1089-1096.

[12] J Onuki, M Koizumi and M Suwa, "Reliability of thick Al wire bonds in IGBT modules for traction motor drives", *IEEE Trans. Advanced Packaging*, vol. 23, no. 1, 2000.

[13] R Amro, "Packaging and interconnection technologies of power devices, Challenges

and future trends", *World academy of science, engineering and technology*, 49, pp. 691-694, 2009.

[14] B Bernoux, R Escoffier, P Jalbaud, J Reynes, E Scheid and J Dorkel, "Power MOSFET R_{DSON} under repetitive avalanche cycling" *IEEE International Symposium on Industrial Electronics,*2009, pp. 2016-2019.

[15] D Sornette, T Magnin and Y Brechet, "The physical origin of the Coffin-Manson Law in low-cycle fatigue", *Europhysics Lett,* 20 (5), pp. 433-438, 1992.

[16] H Cui, "Accelerated temperature cycle test and Coffin-Manson model for electronic packaging", in *proc Reliability and Maintainability Symposium,* 2005, pp. 556-560.

TABLE 1. RESULTS OF REPETITIVE AVALANCHE EXPERIMENTS PERFORMED ON POWER MOSFETS

Device	I_{AV} (A)	P_{AV} (W/mm^2)	E_{AV} (J)	ΔT_J (°C)	NCTF (x10^6)
25 mm^2 in TO-220	230	230	2.6	90	28
25 mm^2 in TO-220	245	245	3.0	95	12
25 mm^2 in TO-220	250	250	3.1	96	2
49 mm^2 in module	400	204	8.0	85	13
49 mm^2 in module	370	188	6.8	77.3	43
58 mm^2 in module	400	172	8.0	72	43
58 mm^2 in module	400	172	8.0	66	59

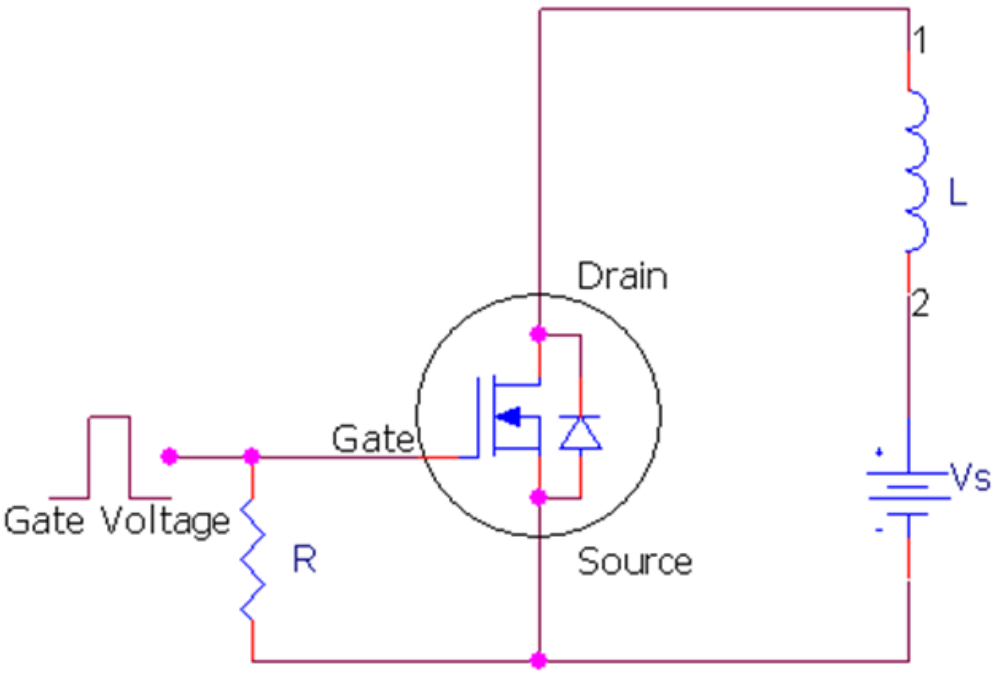

Fig. 1(a). Schematic diagram of a MOSFET driving an inductive load connected to a power supply.

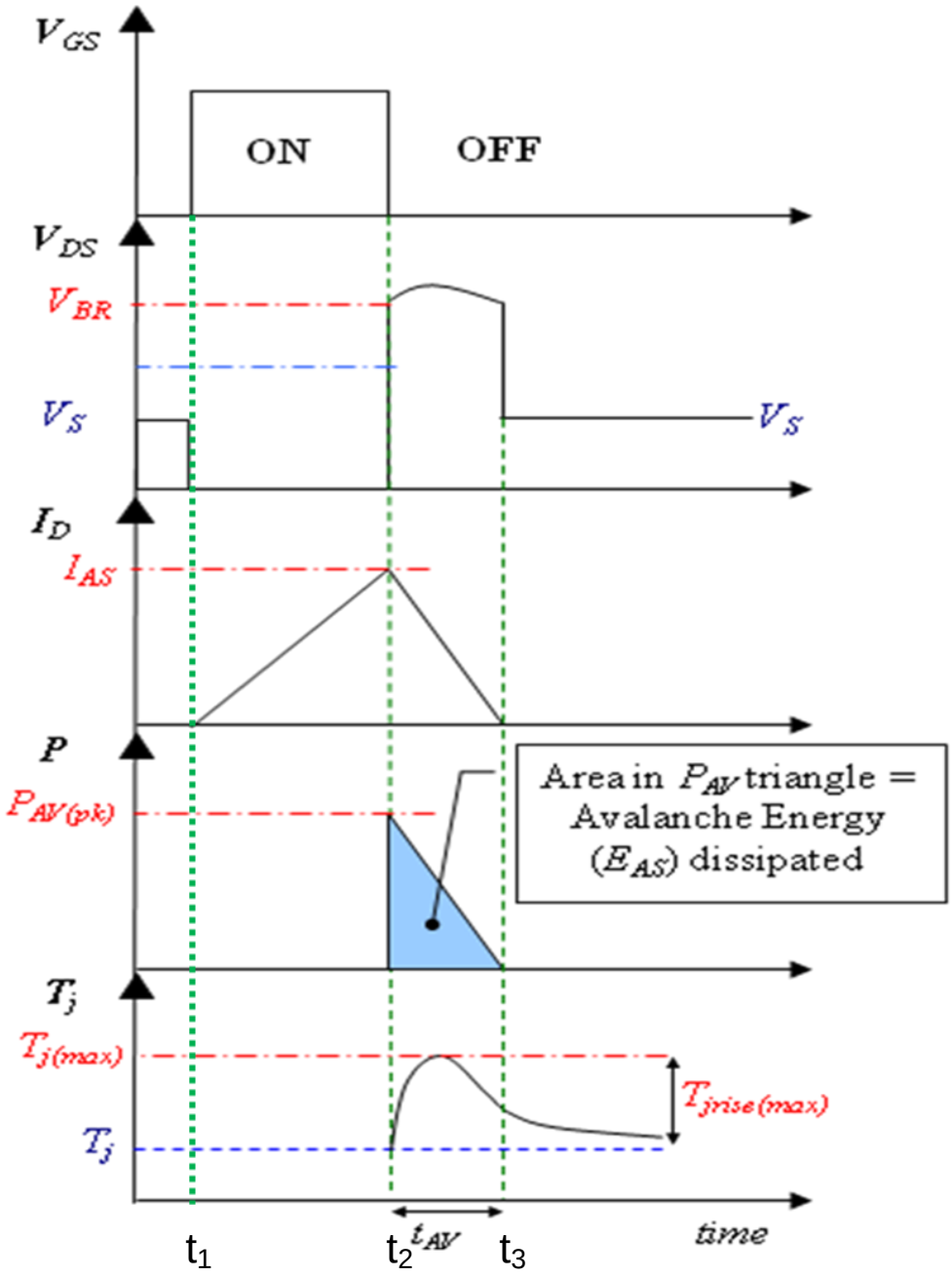

Fig. 1(b). Timing diagrams of the gate voltage, drain voltage, drain current, power and junction temperature showing transient behavior of a MOSFET switch connected to an inductive load. When V_{GS} is high, the V_{DS} falls and I_{DS} ramps up. When the MOSFET is switched off, inductive energy in the inductor is dissipated in the MOSFET by taking V_{DS} to B_{VDSS} as I_{DS} ramps down.

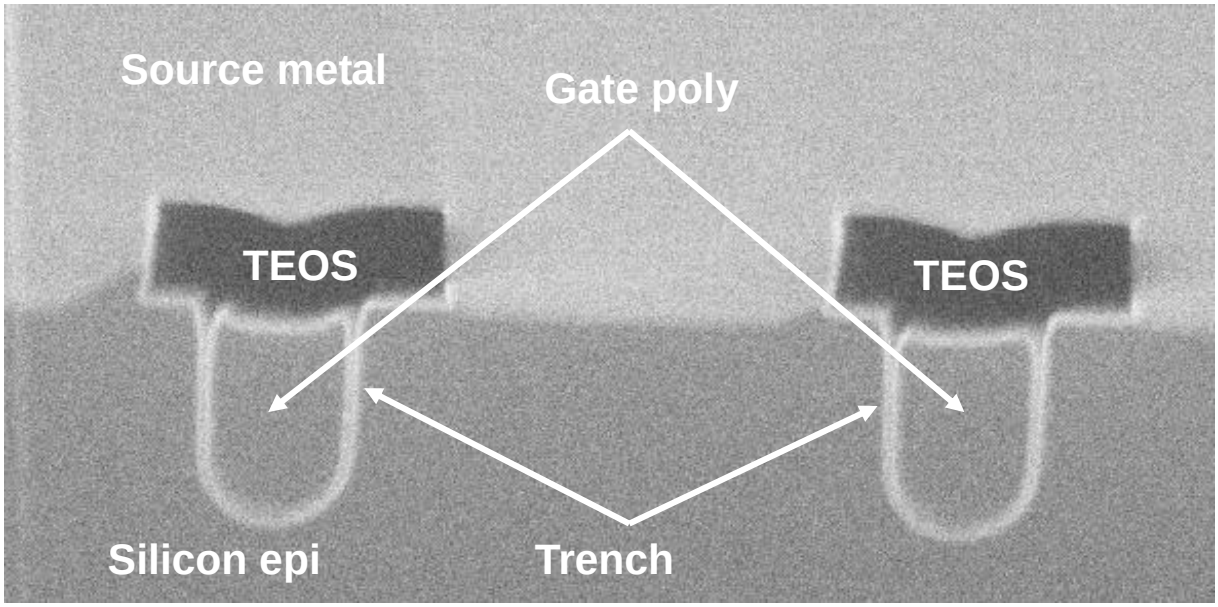

Fig. 2. A cross-sectional image of a trench MOSFET which shows the trenches, the gate polysilicon, the gate dielectric, the TEOS passivation and the source aluminum.

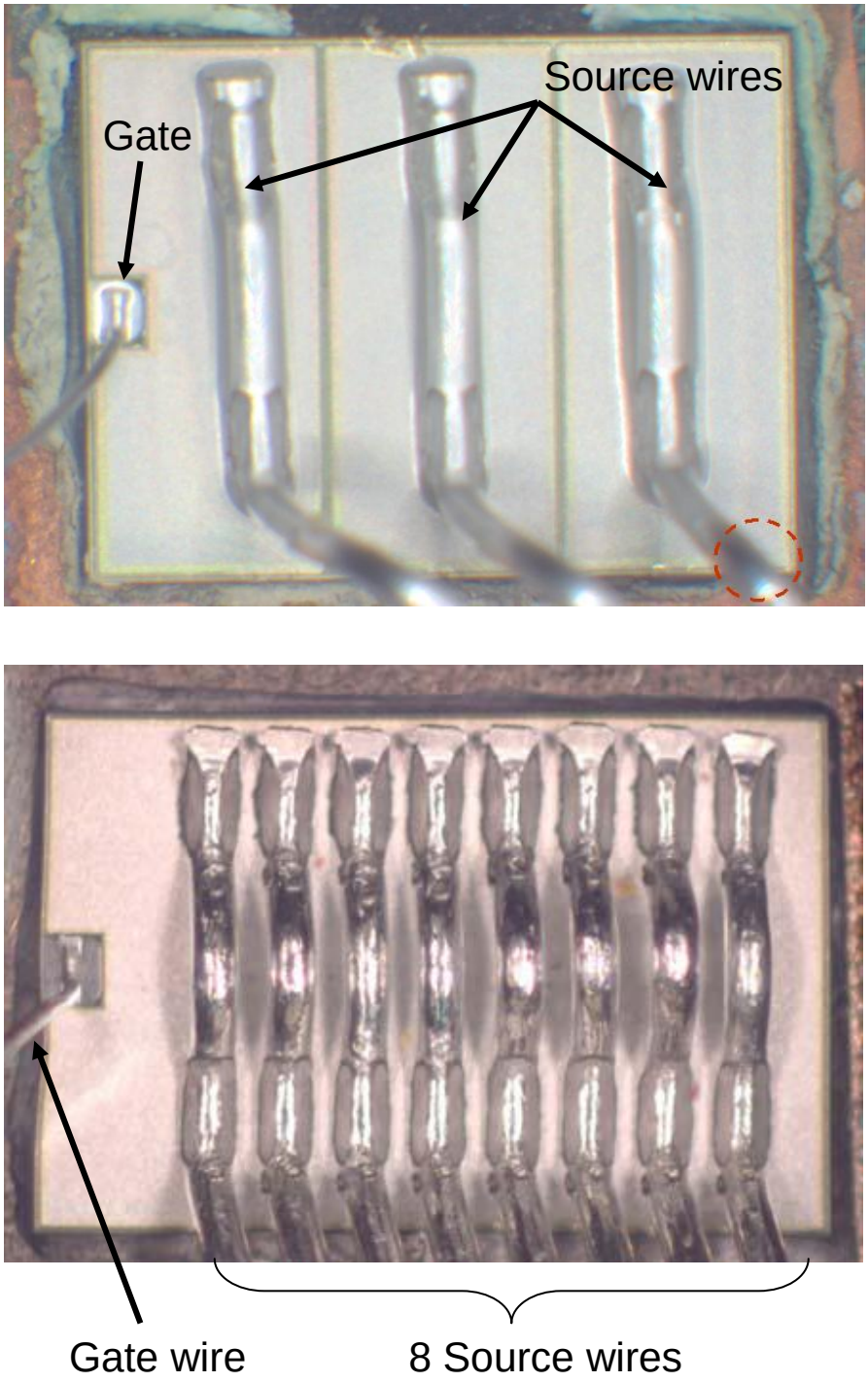

Fig. 3(a). The 25 mm^2 de-capped power MOSFET showing the 3 source wires and the gate wire. (b). The 49 mm^2 de-capped power MOSFET showing the 3 source wires and the gate wire.

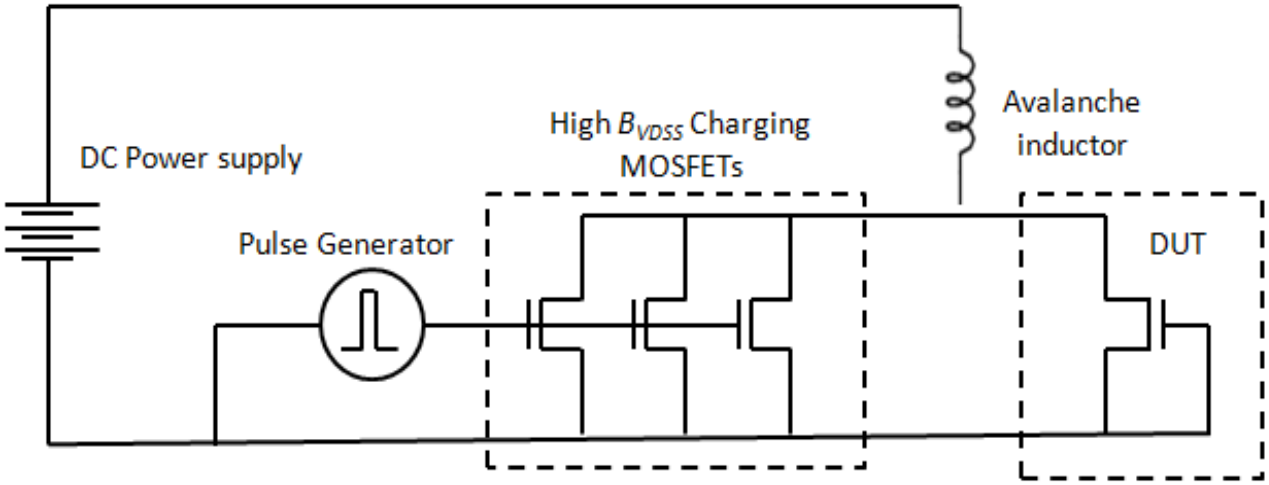

Fig. 4. The custom made repetitive avalanche test equipment showing the pulse generator, the charging MOSFETs, the inductor, the power supply and the DUT.

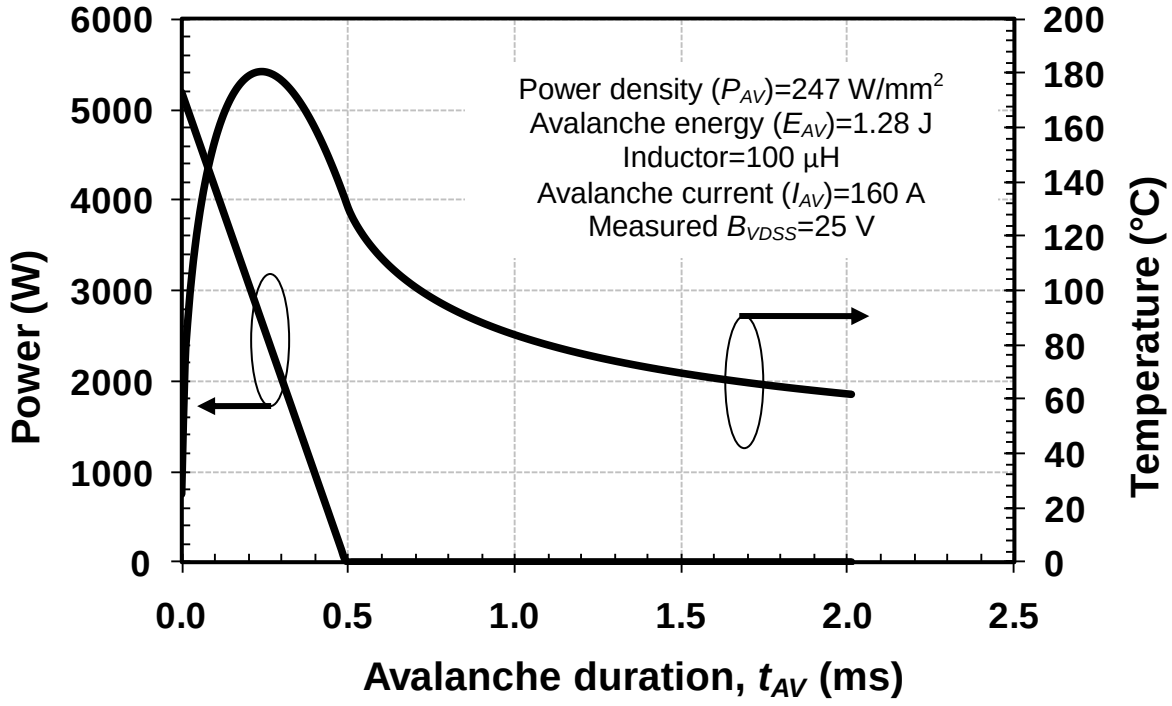

Fig. 5. Avalanche power and junction temperature as a function of the avalanche duration for a 25 mm2 MOSFET. The junction temperature profile is obtained from the empirically derived transient thermal impedance curve.

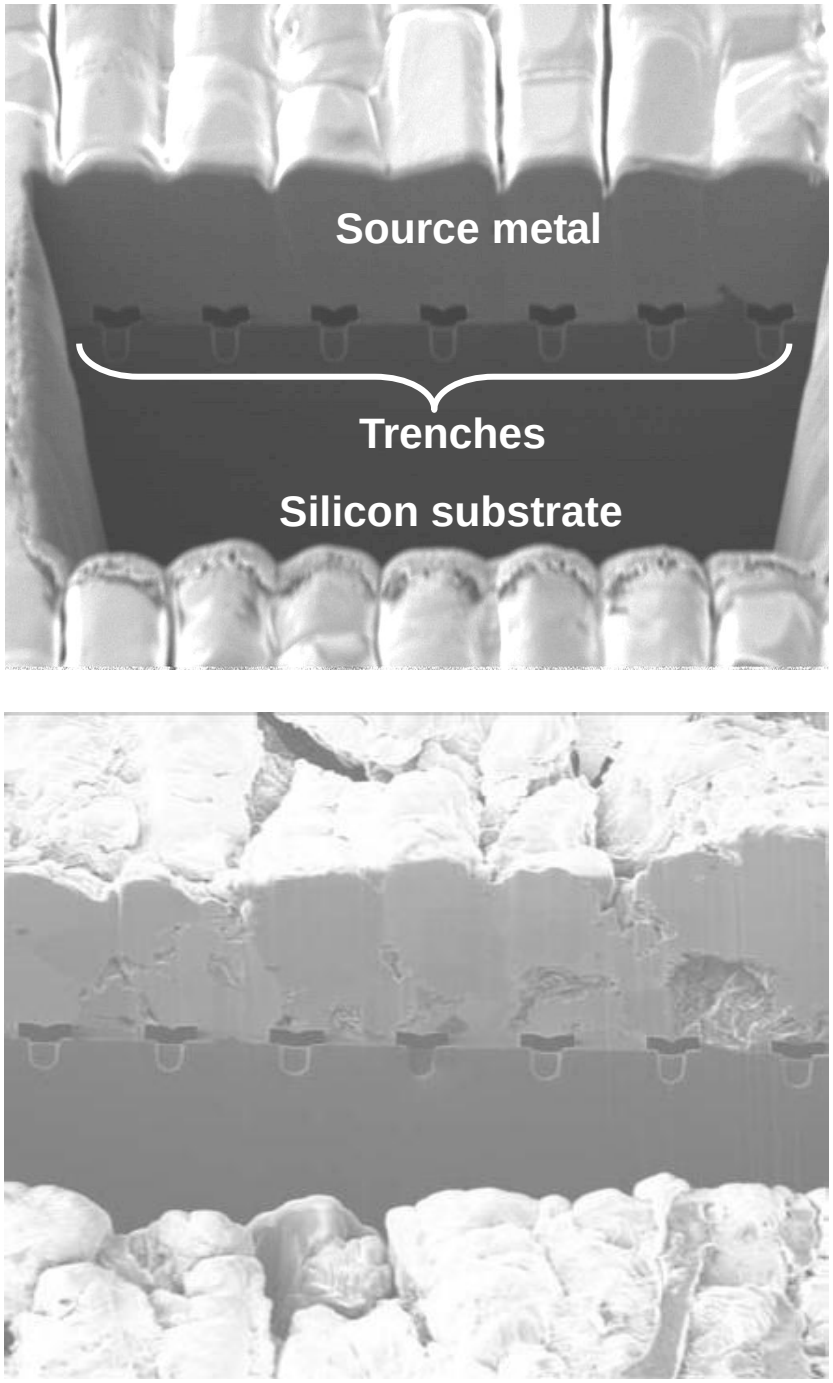

Fig. 6(a). A cross-sectional FIB image of an un-tested power MOSFET showing the cells and source metallization. (b). A cross-sectional image of an identical device that has been through 100 million cycles of repetitive avalanche.

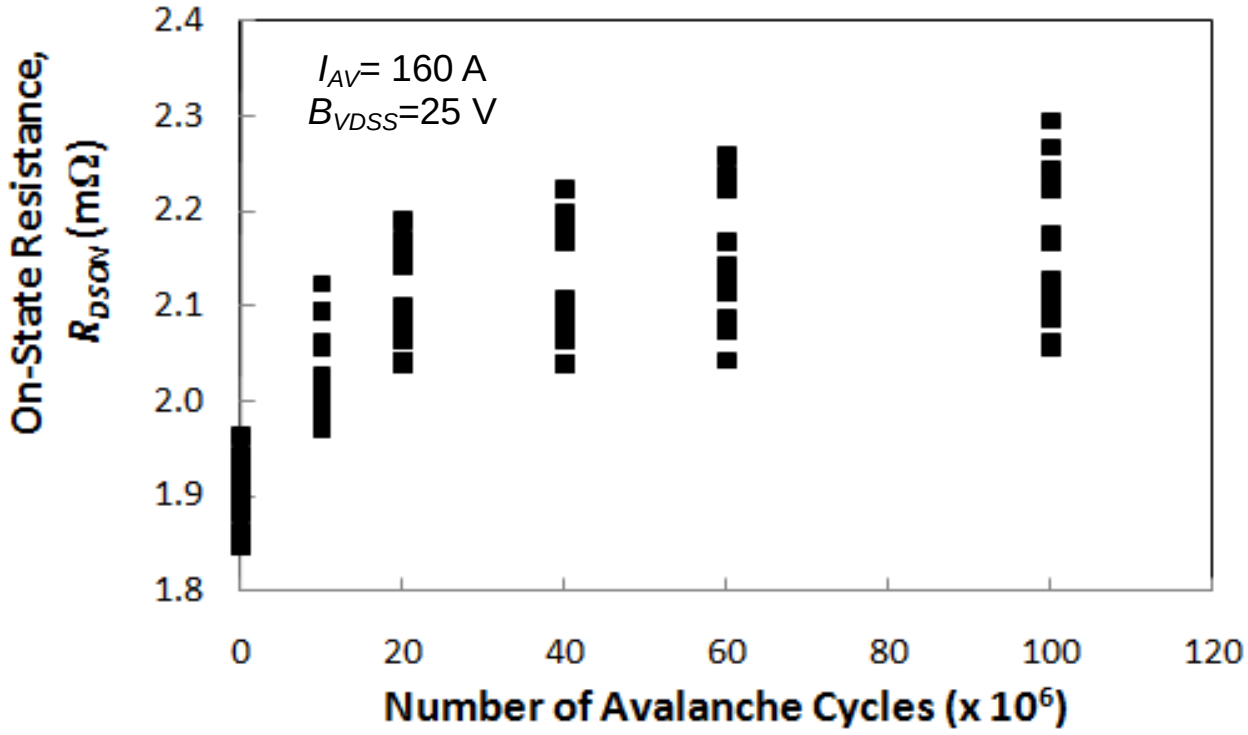

Fig. 7. The R_{DSON} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 µm cell pitch trench devices tested under repetitive UIS. The increase in R_{DSON} is an average of 20% for the MOSFETs and is due to degraded contact resistance between the aluminum source metal and the source wirebonds.

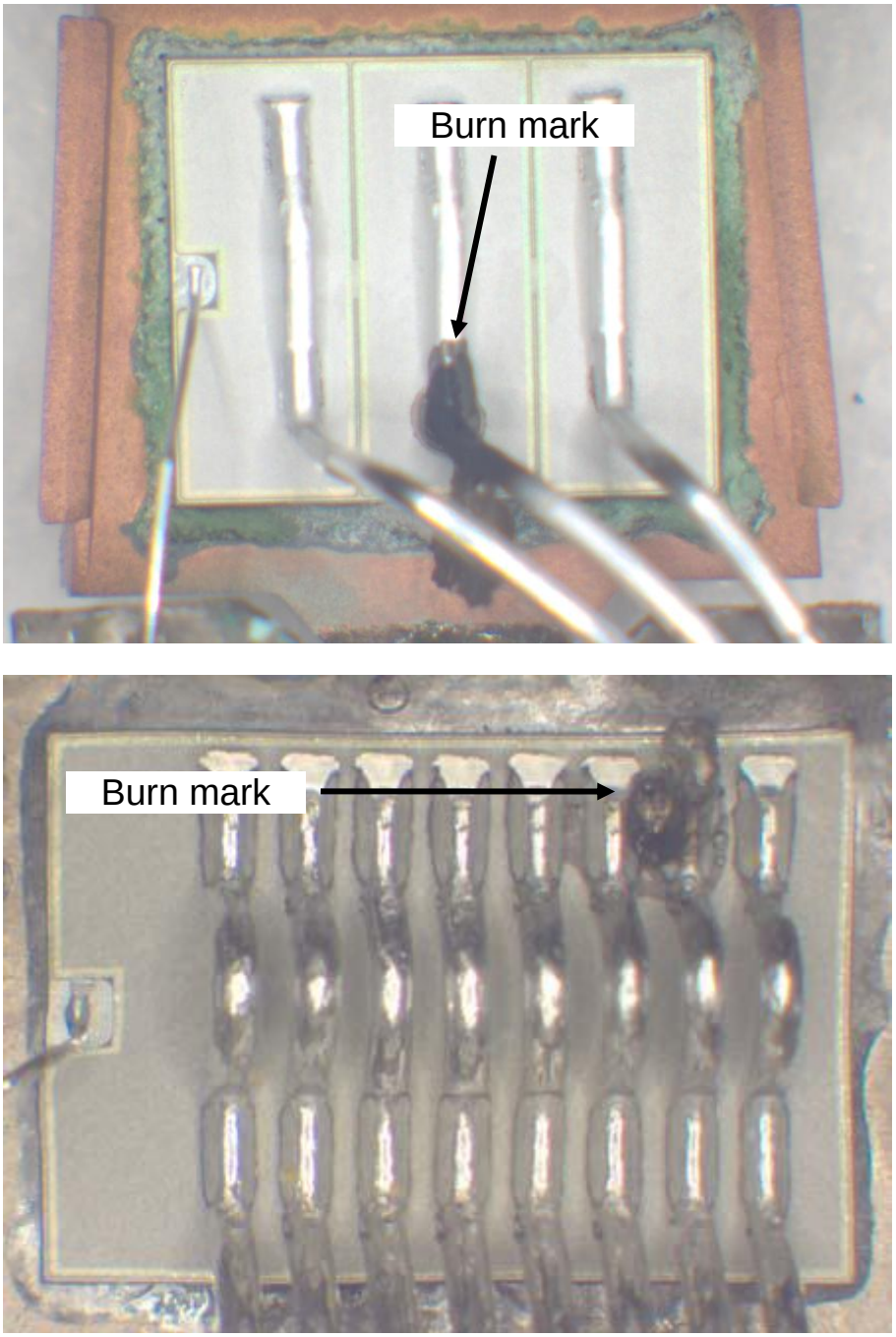

Fig. 8(a). A picture of the de-capped 25 mm^2 MOSFET that has been repetitively avalanched to destruction. The failure signature is wirebond lift-off and a region of melted source metal (b). A picture of the de-capped 25 mm^2 MOSFET that has been repetitively avalanched to destruction.

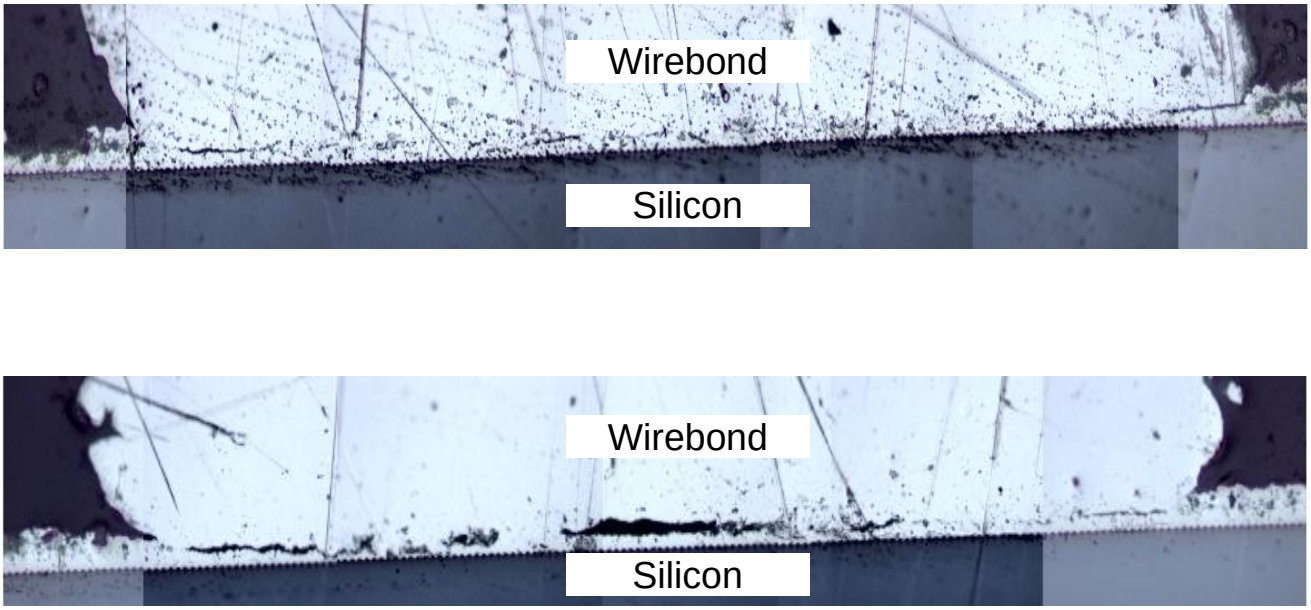

Fig. 9(a). A cross-sectional image of the wirebond to source metal interface for a power MOSFET that has undergone 2 million cycles of repetitive avalanche (b). A picture of the de-capped 25 mm^2 MOSFET that has been repetitively avalanched to destruction showing a similar failure signature as the 25 mm^2 device.

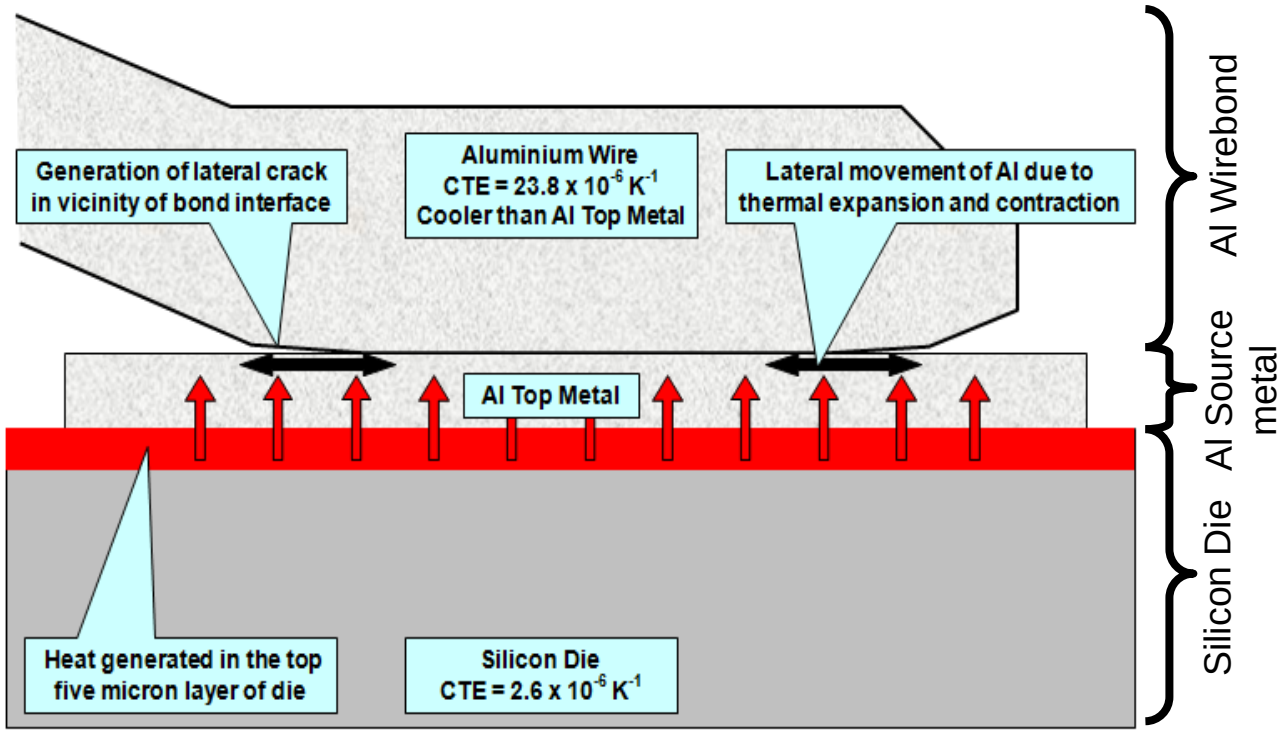

Fig. 10. A schematic representation of the MOSFET cross-section showing the wirebond, source metal and silicon chip interfaces. Differences in the thermal boundary conditions between the source metal and the wirebond causes cyclical mechanical stresses which result in crack generation and propagation along the interface.

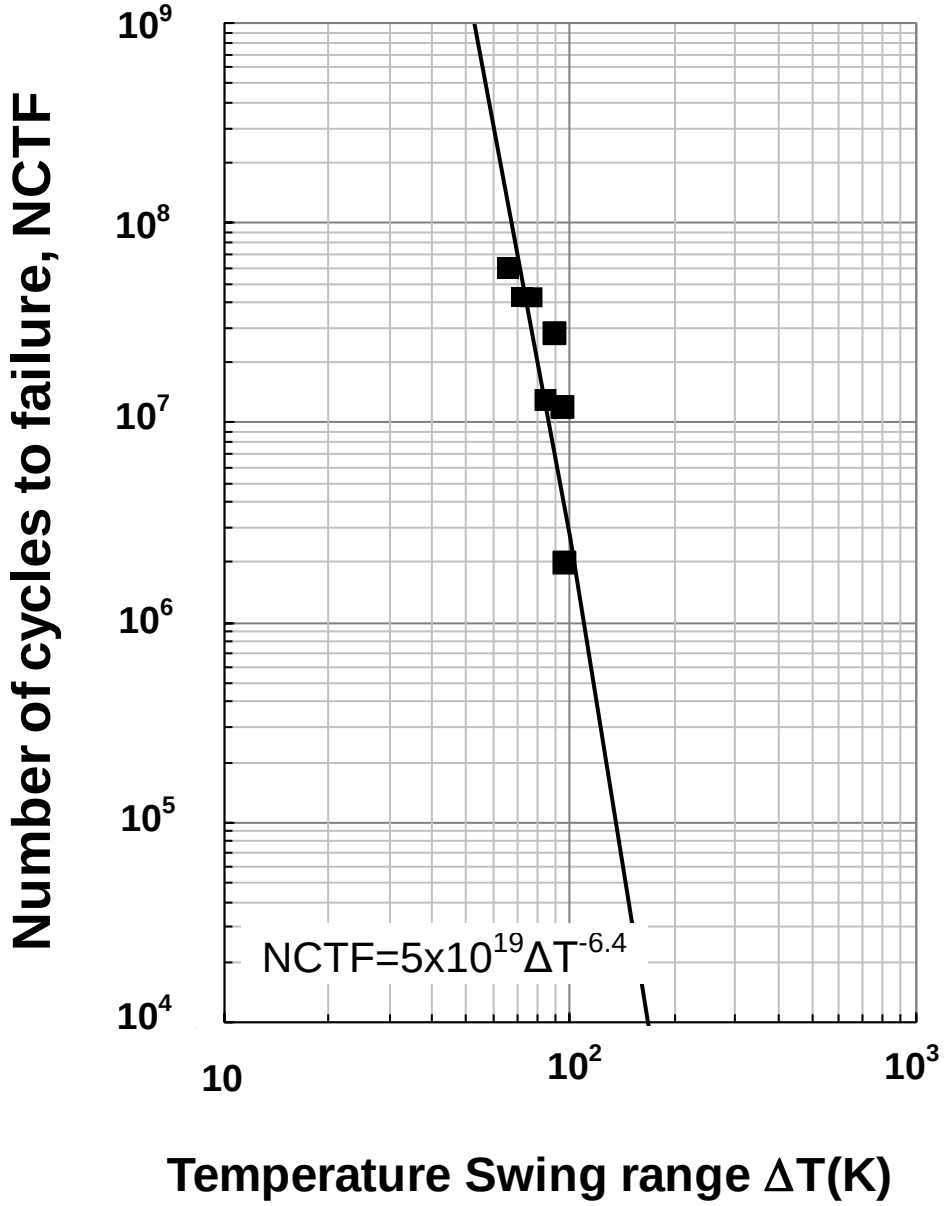

Fig. 11. The number of cycles to failure as a function of the temperature swing calculated from the dissipation of the avalanche pulse. The measurements follow the Coffin-Manson relation.